

A method and system for controlling the operations of a multi-processor system in a programmable fashion that allows tuning of the operational flow including support for hot swapping. A system control register or registers with a plurality of fields are defined to allocate system resources available at I/O ports to anticipated transactions at those ports. The control register(s) fields may include, for each port, the number of direct memory access engines available to support transactions, the number of cache lines available for requested data, the priorities of the anticipated transactions, etc.. One field supports hot swapping wherein the registers, memory and cache contents and status are flushed and stored and the system directory is updated. Also, and the status of data with respect to the swapped assembly is updated to inform the system.